Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A data processing apparatus that has a plurality of reception interface sections which receive same data from a same data sender and processes data, received by said plurality of reception interface sections, in parallel, comprising:

a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock signal and sends said generated sync signal to each of said reception interface sections and said data sender,

wherein each of said reception interface sections receives data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal supplied from said frequency divider, from said data sender according to said sync signal,

wherein each of said reception interface sections includes a communication error processing section which, upon occurrence of an error in said received data by one of said reception interface sections, stops receiving said data, sends a communication error signal to all other of said reception interface sections to stop data reception from said data sender, and requests said data sender to resend data,

wherein each of said reception interface sections includes an arithmetic operation unit, an I/O unit, and a memory bridge that provides data from said arithmetic operation unit to said I/O unit of the respective reception interface section,

wherein said error in said received data is detected by said memory bridge of said one of said reception interface sections, and

wherein said memory bridge of said one of said reception interface sections sends the communication error signal to said other memory bridges of said other reception interface sections.

2. (Original) The data processing apparatus according to claim 1, wherein when an error occurs in part of received data, said communication error processing section of each of said reception interface sections cancels said error-occurred data, and requests said data sender to resend said canceled data.

3. (Original) The data processing apparatus according to claim 1, wherein said data sender sends same serial data, and

when an error occurs in received serial data, said communication error processing section of each of said reception interface sections cancels said error-occurred serial data and serial data received following that error-occurred serial data, and requests said data sender to resend said canceled serial data.

4. (Original) The data processing apparatus according to claim 1, wherein said data sender sends said data packet by packet with a sequence number affixed to each packet, and

when an error occurs in data of the received packet, said communication error processing section of each of said reception interface sections requests said data sender to resend data packet by packet based on said sequence number affixed to each packet received.

5. (Canceled)

6. (Previously Presented) A data processing apparatus that has a transmission interface section which transmits transmission data to a plurality of data receivers at a same timing, comprising:

a frequency divider which generates a sync signal by dividing a frequency of a predetermined clock signal and sends said generated sync signal to said transmission interface section and said plurality of data receivers,

wherein said transmission interface section generates packet data by dividing said transmission data to data of a data length shorter than one period length of said sync signal supplied from said frequency divider and sends individual pieces of packet data generated to said plurality of data receivers at the same timing in synchronism with said clock signal.

7. (Previously Presented) A data processing method that performs parallel processing of data received by a plurality of reception interface sections which receive same data from a same data sender and comprises:

a frequency division step of generating a sync signal by dividing a frequency of a predetermined clock signal and sending said generated sync signal to each of said reception interface sections and said data sender;

a data reception step of receiving data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal generated in said frequency division step, from said data sender at each of said plurality of reception interface sections according to said sync signal;

an error detection step of detecting an error in said received data by one of said reception interface sections; and

an error information output step of outputting information on said detected error by said one of said reception interface sections to all other of said reception interface sections,

wherein each of said reception interface sections includes an arithmetic operation unit, an I/O unit, and a memory bridge that provides data from said arithmetic operation unit to said I/O unit of said respective reception interface section,

wherein said error detection step comprises detecting said error in said received data by said memory bridge of said one of said reception interface sections, and

wherein said error information output step comprises sending, by said memory bridge of said one of said reception interface sections, said information on said detected error to said other memory bridges of said other reception interface sections.

8. (Currently Amended) The data processing method according to claim 7, wherein said error information output step [[are]] is executed according to said sync signal.

9. (Original) The data processing method according to claim 8, further comprising:

an error information reception step of receiving error information, output from said other reception interface sections, at said one of said reception interface sections; and

a data resend requesting step of requesting said data sender to resend data in at least one of a case where an error is detected at said error detection step and a case where error information is received at said error information reception step.

10. (Original) The data processing method according to claim 9, further comprising:

a data cancellation step of canceling data; and

a data reception stopping step of stopping data reception, and wherein

said data cancellation step and said data reception stopping step are executed in at least one of a case where an error is detected at said error detection step and a case where error information is received at said error information reception step, and

said data resend requesting step requests resending of data canceled at said data cancellation step.

11. (Original) The data processing method according to claim 10, wherein said data cancellation step is executed according to said sync signal.

12. (Previously Presented) A computer readable medium having thereon a computer program, which when executed, performs parallel processing of data received by a plurality of reception interface sections which receive same data from a same data sender and allows a computer to execute:

a frequency division step of generating a sync signal by dividing a frequency of a predetermined clock signal and sending said generated sync signal to each of said reception interface sections and said data sender;

a data reception step of receiving data, which is divided by said data sender to data of a data length shorter than one period length of said sync signal generated in said frequency division step, from said data sender at each of said plurality of reception interface sections according to said sync signal;

an error detection step of detecting an error in said received data by one of said reception interface sections; and

an error information output step of outputting information on said detected error by said one of said reception interface sections to all other of said reception interface sections,

wherein each of said reception interface sections includes an arithmetic operation unit, an I/O unit, and a memory bridge that provides data from said arithmetic operation unit to said I/O unit of said respective reception interface section,

wherein said error detection step comprises detecting said error in said received data by said memory bridge of said one of said reception interface sections, and

wherein said error information output step comprises sending, by said memory bridge of said one of said reception interface sections, said information on said detected error to said other memory bridges of said other reception interface sections.

13. (Currently Amended) The computer readable medium according to claim 12, wherein said error information output step [[are]] is executed according to said sync signal.

14. (Previously Presented) The computer readable medium according to claim 13, wherein said computer is allowed to further execute:

an error information reception step of receiving error information, output from said other reception interface sections, at said one of said reception interface sections; and

a data resend requesting step of requesting said data sender to resend data in at least one of a case where an error is detected at said error detection step and a case where error information is received at said error information reception step.

15. (Previously Presented) The computer readable medium according to claim 14, wherein said computer is allowed to further execute:

a data cancellation step of canceling data; and

a data reception stopping step of stopping data reception, and

said data cancellation step and said data reception stopping step are executed in at least one of a case where an error is detected at said error detection step and a case where error information is received at said error information reception step, and

said data resend requesting step requests resending of data canceled at said data cancellation step.

16. (Previously Presented) The computer readable medium according to claim 15, wherein said data cancellation step is executed according to said sync signal.

17. (Previously Presented) The data processing apparatus according to claim 1, wherein said memory bridge of said one of said reception interface sections sends the

communication error signal to said other memory bridges of said other reception interface sections as an open drain signal.

18. (Previously Presented) The data processing method according to claim 7, wherein, in said error information output step, said memory bridge of said one of said reception interface sections sends the communication error signal to said other memory bridges of said other reception interface sections as an open drain signal.

19. (Previously Presented) The computer readable medium according to claim 12, wherein, in said error information output step, said memory bridge of said one of said reception interface sections sends the communication error signal to said other memory bridges of said other reception interface sections as an open drain signal.

20. (Currently Amended) The data processing apparatus according to claim 1, ~~wherein a difference occurs in a timing that the plurality of reception interface sections receives the same data, and wherein the plurality of reception interface sections receive the same data within a same period of said sync signal~~ further comprising:

a transaction layer that receives the communication error signal output from the communication error processing section;

an internal circuit section; and

a synchronization buffer that exchanges data between the transaction layer and the internal circuit section,

wherein the internal circuit section acquires data held in the synchronization buffer at a timing synchronous with said sync signal and sends the acquired data to a processor external to the data processing apparatus.

21. (Currently Amended) The data processing method according to claim 7, further comprising:

~~receiving the same data at different points in time by the plurality of reception interface sections,~~

~~wherein the plurality of reception interface sections receive the same data within a same period of said sync signal~~

receiving, by a transaction layer, a communication error signal output in the error information output step;

exchanging data, by a synchronization buffer, between a transaction layer and an internal circuit section, wherein the internal circuit section acquires data held in the synchronization buffer at a timing synchronous with said sync signal; and

sending the acquired data by the internal circuit section to a processor external to the data processing apparatus.